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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/686,327 | 10/11/2000 | Serge F. Fruhauf | 00AU11952023 | 4726 |

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| EXAMINER | |
|---|---|
| LE, THIEN MINH | |
| ART UNIT | PAPER NUMBER |
| 2876 | |

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/686,327 | FRUHAUF ET AL. | |
| | Examiner | Art Unit | |
| | Thien M. Le | 2876 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

The information disclosure statements filed on 6/12/2002 and 10/11/2000 have been entered. Claims 1-33 are presented for examination.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,439,464 (herein after referred to as the '464 patent). Although the conflicting claims are not identical, they are not patentably distinct from each other because recite the same limitations.

Regarding claim 1, claim 1 of the '464 patent discloses:

1 A dual mode integrated circuit (IC) for operating in an ISO mode in accordance with International Standards Organization

7816 (ISO 7816) protocol, and a USB mode in accordance with a Universal Serial Bus protocol, the dual-mode IC comprising:

a microprocessor;

a switching block connected to the microprocessor;

an external interface connected to the switching block and comprising a voltage supply pad, a reference voltage pad, a reset pad, a clock pad and an input/output pad in accordance with the ISO 7816 protocol, and a D-plus pad and a D-minus pad in accordance with the USB protocol;

and a mode configuration circuit connected to the switching block for configuring the dual-mode IC in one of the ISO and USB modes based upon a signal on at least one of the D-plus and D-minus pads.

As can be seen, claim 1 of the '464 patent recites a microprocessor, a voltage supply pad, a ground pad, a set of ISO 7816 pads, and a set of non-ISO pads; and thus embraces all limitations set forth in claim 1 of the instant invention. Thus, the patent protections have been granted to the earlier patented application.

Similarly, claim 2 is rejected in view of claim 2 of the '464 patent. Claim 2 of the '464 patent recites:

2. The dual-mode IC according to claim 1 wherein the mode configuration circuit comprises: a USB mode detector connected to at least the D-minus pad for detecting a USB condition; and a

latching circuit connected to the switching block and receiving an output from the USB mode detector.

As can be seen, selecting one mode would effectively diabling the other mode of operation.

Similarly claims 3-33 of the instant invention are rejected in view of claims 3-33 of the '464 patent in that the claims recites:

3. The dual-mode IC according to claim 2 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if a USB condition is not detected by the USB mode detector.

4. The dual-mode IC according to claim 2 wherein the USB mode detector is also connected to the D-plus pad.

5. The dual-mode IC according to claim 2 wherein the mode configuration circuit further comprises an ISO mode detector connected between the reset pad and the latching circuit for detecting an ISO condition.

6. The dual-mode IC according to claim 5 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if an ISO condition is detected by the ISO mode detector.

7. The dual-mode IC according to claim 2 further comprising a control register connected to the latching circuit for storing a mode configuration indicator.

8. The dual-mode IC according to claim 2 further comprising a USB voltage detector connected between the voltage supply pad and the latching circuit to detect a USB voltage supply.

9. The dual-mode IC according to claim 1 wherein the mode configuration circuit configures the dual-mode IC to operate in one of the ISO and USB modes while disabling the other of the ISO and USB modes.

10. The dual-mode IC according to claim 9 wherein the reset, clock and input/output pads are disabled when the dual-mode IC is configured in the non-ISO mode, and the D-plus and D-minus pads are disabled when the dual-mode IC is configured in the ISO mode.

11. A dual-mode smart card for operating in an ISO mode in accordance with International Standards Organization 7816 (ISO 7816) protocol, and a USB mode in accordance with a Universal Serial Bus protocol, the dual-mode smart card comprising: a card body; and a dual-mode integrated circuit (IC) carried by the card body and comprising an external interface including a voltage supply pad, a reference voltage pad, a first set of pads including a reset pad, a clock pad and an input/output pad in accordance with the ISO 7816 protocol, and a second set of pads including a D-plus pad and a D-minus pad in accordance with the USB protocol, and a mode configuration circuit for configuring the dual-mode IC in one of the ISO and USB modes and comprising a USB mode detector connected to at least the D-minus pad for detecting a USB condition, and a latching circuit connected to the USB mode detector.

12. The dual-mode smart card according to claim 11 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if a USB condition is not detected by the USB mode detector.

13. The dual-mode smart card according to claim 11 wherein the USB mode detector is also connected to the D-plus pad.

14. The dual-mode smart card according to claim 11 wherein the dual mode IC further comprises an ISO mode detector connected between the reset pad and the latching circuit for detecting an ISO condition.

15. The dual-mode smart card according to claim 14 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if an ISO condition is detected by the ISO mode detector.

16. The dual-mode smart card according to claim 11 wherein the dual-mode IC further comprises a control register connected to the latching circuit for storing a mode configuration indicator.

17. The dual-mode smart card according to claim 11 wherein the mode configuration circuit further comprises a USB voltage

detector connected between the voltage supply pad and the latching circuit to detect a USB voltage supply.

18. The dual-mode smart card according to claim 11 wherein the mode configuration circuit configures the dual-mode IC to operate in one of the ISO and non-ISO modes while disabling the other of the ISO and non-ISO modes.

19. The dual-mode smart card according to claim 18 wherein the reset, clock and input/output pads are disabled when the dual-mode IC is configured in the USB mode, and the D-plus and D-minus pads are disabled when the dual-mode IC is configured in the ISO mode.

20. A dual-mode smart card system for operating in an ISO mode in accordance with International Standards Organization 7816 (ISO 7816) protocol, and a USB mode in accordance with a Universal Serial Bus protocol, the dual-mode smart card system comprising: a dual-mode smart card including a dual-mode integrated circuit (IC) comprising an external interface including a voltage supply pad, a reference voltage pad, a reset pad, a clock pad and an input/output pad in accordance with the ISO 7816 protocol, and a D-plus pad and a D-minus pad in accordance with the USB protocol, and a mode configuration circuit for configuring the dual-mode IC in one of the ISO mode and the USB mode and comprising a USB mode detector connected to the D- minus pad, and a latching circuit connected to the USB mode detector; at least one of an ISO-compliant smart card reader and a USB-compliant smart card reader for reading the dual-mode smart card, the ISO-compliant smart card reader including an ISO interface having a plurality of contacts for respectively mating with the voltage supply pad, the reference voltage pad, the reset pad, the clock pad and the input/output pad in accordance with the ISO 7816 protocol, and the USB-compliant smart card reader including a USB interface having a plurality of contacts for respectively mating with the voltage supply pad, the reference voltage pad, the D-plus pad and the D-minus pad in accordance with the USB protocol.

21. The dual-mode smart card system according to claim 20 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if a USB condition is not detected by the USB mode detector.

22. The dual-mode smart card system according to claim 20 wherein the USB mode detector is also connected to the D-plus pad.

23. The dual-mode smart card system according to claim 20 wherein the mode configuration circuit further comprises an ISO mode detector connected between the reset pad and the latching circuit for detecting an ISO condition.

24. The dual-mode smart card system according to claim 23 wherein the mode configuration circuit configures the dual-mode IC in the USB mode if a USB condition is detected by the USB mode detector, and configures the dual-mode IC in the ISO mode if an ISO condition is detected by the ISO mode detector.

25. The dual-mode smart card system according to claim 20 wherein the mode configuration circuit further comprises a control register connected to the latching circuit for storing a mode configuration indicator.

26. The dual-mode smart card system according to claim 20 wherein the mode configuration circuit further comprises a USB voltage detector connected between the voltage supply pad and the latching circuit to detect a USB voltage supply.

27. The dual-mode smart card system according to claim 20 wherein the mode configuration circuit configures the dual-mode IC to operate in one of the ISO and USB modes while disabling the other of the ISO and USB modes.

28. The dual-mode smart card system according to claim 27 wherein the reset, clock and input/output pads are disabled when the dual-mode IC is configured in the USB mode, and the D-plus and D-minus pads are disabled when the dual-mode IC is configured in the ISO mode.

29. A method of operating a dual-mode integrated circuit (IC) in an ISO mode in accordance with International Standards Organization 7816 (ISO 7816) protocol, and a USB mode in accordance with a Universal Serial Bus protocol, the dual-mode IC including an external interface having a voltage supply pad, a first set of pads including a reset pad, a clock pad and an input/output pad in accordance with the ISO protocol, and a second set of pads including a D-plus pad and a D-minus pad in accordance with the USB protocol, the method comprising: detecting whether a USB-mode condition exists on at least one pad of the second set of pads; configuring the dual-mode IC in one of

the ISO mode and the USB mode based upon the detection; and disabling one of the first and second set of pads based upon the configuration.

30. The method according to claim 29 wherein detecting whether the USB-mode condition exists on at least one pad of the second set of pads comprises detecting whether the USB-mode condition exists during a power-on-reset of the dual-mode IC.

31. The method according to claim 29 wherein detecting whether the USB-mode condition exists on at least one pad of the second set of pads comprises detecting whether the USB-mode condition exists on the D-minus pad.

32. The method according to claim 29 wherein detecting whether the USB-mode condition exists on at least one pad of the second set of pads comprises detecting whether the USB-mode condition exists on the D-plus pad and the D-minus pad.

33. The method according to claim 29 wherein the dual-mode IC is configured in the USB mode when the USB-mode condition is detected, and configured in the ISO mode when the USB-mode condition is not detected.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien M. Le whose telephone number is (571) 272-2396. The examiner can normally be reached on Monday - Friday from 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Le, Thien Minh**
**Primary Examiner**
**Art Unit 2876**
**May 27, 2004**